REMARKS

Amended Claims

Claims 1, 22, 27, 45, 60, 75, 79, 94, 96, 98 and 99 are amended herein. Claims 11-12, 34-35, 52-53, 67-68 and 86-87 are cancelled.

Interview Summary

In a telephonic conversations on January 10, 2008, and on January 14, 2008, between Examiner Hetul B. Patel and the below-signed attorney, Andrew C. Walseth, the Examiner and Applicant's Representative discussed the Present Application, the Final Office Action mailed November 1, 2007, and the Response to Final Office Action mailed on January 2, 2008.

Applicant and the Examiner discussed the pending claims and cited references. Applicant contended that the references did not teach or suggest all elements of the claims and that the Specification did clearly define and enable one of ordinary skill in the art to make and use the claimed invention, contrary to the Examiner's assertion.

In particular, as discussed in the Response to Final Office Action mailed on January 2, 2008, Applicant continued to respectfully contend that the Final Office Action mischaracterize the cited references. In particular, the Office Action asserts that Zitlaw et al. (U.S. Patent Publication No. 2004-0128425) and McClain (U.S. Patent No. 7,058,779) both teach systems having a processor coupled to volatile and non-volatile memory devices that, as a whole, present themselves as a synchronous memory device through an external synchronous memory interface and therefore function as a unitary synchronous memory device. Applicant again acknowledged that, while Zitlaw et al. and McClain do indeed have controllers or processors coupled to both volatile and non-volatile memory devices, the references only purport to present conventional computer systems. As such, they do not disclose that the systems have an external synchronous memory interface or that the systems present themselves externally as a memory device through this external synchronous memory interface. *See, e.g.,* Zitlaw et al., Abstract, Figures 1A and 1B, Paragraphs [0008]-[0009] and [0036]-[0037]; McClain, Figures 1 and 2, Abstract, and Column 3, Line 20 to Column 5, Line 6. Thus, the systems of Zitlaw et al. and McClain, while having both volatile and non-volatile memory devices, do not present themselves externally as unitary synchronous memory devices having an external synchronous memory device interface, and therefore cannot be used in larger systems as replacements for synchronous memory device

components. Therefore, there is no teaching in the references, either expressly or inherently, that the systems of Zitlaw et al. and McClain are capable of presenting themselves externally through an external synchronous memory interface as a unitary synchronous memory device. Applicant also contended that McCormack et al. (U.S. Patent No. 5,781,201), Widdup (U.S. Patent No. 6,651,148). Wallace et al. (U.S. Patent No. 6,628, 537), Meyer (U.S. Patent No. 4,065,862), Bartoli et al. (U.S. Patent No. 6,442,068), and the 'Background of Invention' (BOI) section of the present application did not teach or suggest the missing elements and thus the rejection of the claims under both 35 U.S.C. § 102(e) and § 103(a) should be withdrawn.

Applicant also contended that the disclosure did teach "an external synchronous memory interface" and are detailed in at least Paragraphs [0007]-[0009], [0011]-[0017], [0023], [0030]-[0032], [0035], [0038], [0040]-[0042] and [0044]-[0046] and Figures 1-3B of the Present Application. Applicant further respectfully noted that the Present Application is titled "NON-VOLATILE MEMORY WITH SYNCHRONOUS DRAM INTERFACE". Applicant specifically notes that the Specification depicts and refers to unitary memory devices and, as such, contrary to the Examiner's assertion, the synchronous memory interface 130, 216, 322 couples the memory device 100, 204, 304 to external devices and systems and present synchronous memory interface to the systems they are inserted into (*See,* Figures 1, 2, 3A and 3B, memory device elements 100, 204, and 304, and synchronous memory interface elements 130, 216, 322; and Paragraphs [0030], [0038], and [0040]-[0041]). Applicant also noted, that literal disclosure and definition of each and every claim term is not required, as stated in MPEP §2111, §2111.01 and §2173.05(a) and that claim terms are to be given their plain meaning as the would be interpreted by those skilled in the art. Applicant further noted that with regard to the written description and enablement requirement, a specification is presumed enabled unless specific reasons are given to doubt enablement, and that the burden is on the Examiner to establish a prima facie case of non-enablement under 35 U.S.C. §112, 1st Paragraph or lack of antecedent basis for the claim term. (*See*, MPEP §2163 (III)(A), §2163.02. and §2163.04.) Applicant also noted that MPEP §2163.02 states that the "objective standard for determining compliance with the written description requirement is, "does the description clearly allow persons of ordinary skill in the art to recognize that he or she invented what is claimed," and "The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement."

As such, Applicant maintained that the rejection of claims 1-99 under 35 U.S.C. § 112, second paragraph should be withdrawn as the Specification of the Present Application and claims 1-99, clearly define and enable one of ordinary skill in the art to make and use the claimed invention .

After consideration, the Examiner agreed with Applicant that an external synchronous memory interface is disclosed and that the Examiner would withdraw the rejection of claims 1-99 under 35 U.S.C. § 112, second paragraph. The Examiner also indicated that while he did not agree with Applicant on the teachings of the cited references, that Applicant's arguments did indicate that their applicability may not be directly appropriate.

Applicant believes the foregoing interview summary accurately reflects the substance and scope of the interviews and requests notification if the Examiner disagrees with the accuracy or completeness of the interview summary.

Newly Cited References

The Examiner recited the new references Stobbs et al. (U.S. Patent Publication No. 2004-0039871) and Charlier et al. (U.S. Patent Publication No. 2002-0114211) as teaching or suggesting the claimed invention. Applicant respectfully disagrees with the Examiner and contends that the newly cited references of Stobbs et al. (U.S. Patent Publication No. 2004-0039871) and Charlier et al. (U.S. Patent Publication No. 2002-0114211) relayed to Applicant in the Examiner interview of January 14, 2008, do not teach or suggest the claimed invention.

Applicant respectfully maintains that Stobbs et al. discloses a magnetic MRAM memory device 100 designed to replace an asynchronous non-volatile memory device (an asynchronous Flash memory device, such as that holding the BIOS) in a system. In this, as the MRAM memory device is slower even than the relatively slow Flash memory device, it incorporates a internal controller 172 and buffer memory 182. As such, Applicant respectfully maintains that it does not disclose or suggest a non-volatile memory device adapted to present itself externally as a single volatile memory device through an external synchronous memory interface or an SDRAM memory interface, but a slow high density non-volatile memory device (the MRAM memory device) that is designed to mimic and replace another non-volatile memory (the Flash memory device) utilizing an asynchronous memory interface. *See,* Stobbs et al., Figures 1-3; Paragraphs [0007]-[0012], [0020], and [0028]-[0033].

Applicant therefore respectfully continues to submit that Stobbs et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, an external synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the external synchronous interface or SDRAM memory interface as a single volatile synchronous memory device, as maintained by the Examiner. Applicant thus respectfully submits that Stobbs et al. does not teach or suggest all elements of the Applicant's claimed invention.

Applicant respectfully maintains that Charlier et al. discloses a Flash EEPROM memory device wrapper for interfacing asynchronous Flash EEPROM memories with systems and CPUs having synchronous memory bus to allow the asynchronous Flash EEPROM memory device to behave like a synchronous memory. In particular, Charlier et al. discloses that the asynchronous Flash EEPROM memory device and the Flash EEPROM memory device wrapper are particularly useful in developing systems in that Flash EEPROM memory devices typically require their own interfaces/bus to the system/CPU and handling routines. As such, they are hard to replace with RAM or ROM devices once the system has been developed or is altered while in service. *See,* Charlier et al., Figure 2; Paragraphs [0002]-[0005] and [0021]-[0023].

In this Charlier et al. discloses that the device does not operate at full RAM speed and is not a transparent replacement for a synchronous RAM device. In particular, Charlier et al. does not disclose or suggest a buffer memory to buffer reads and writes, and as such, while the Flash EEPROM memory 5 is controlled by the state machine 9 for synchronous read, write, and erase operations, the CPU is made to wait while the state machine/Flash EEPROM is busy, such as while conducting a write or erase operation. *See,* Charlier et al., Paragraph [0024]. Applicant therefore maintains that Charlier et al. does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, an external synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the external synchronous interface or SDRAM memory interface as a single volatile synchronous memory

device, as maintained by the Examiner. Applicant thus respectfully submits that Stobbs et al. does not teach or suggest all elements of the Applicant's claimed invention.

Applicant also respectfully maintains that neither Stobbs et al. nor Charlier et al. disclose or suggest mimicking the full speed read and write speed of a volatile RAM memory device or that the memory interface is a SDRAM interface, DDR interface, DDR2 interface, GDDR interface, GDDR2 interface, or a RDRAM interface memory interface.

In contrast, Applicant has taught and claimed devices that present a controller, an external synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays as a single synchronous memory device that can be used as a direct replacement for volatile synchronous memory devices. In this, the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a unitary volatile synchronous memory device. *See, e.g.,* Specification, the memory devices 100, 204, 304 of Figures 1, 2, and 3A-3B; paragraph 0023 ("..High density non-volatile memory subsystems and devices of the present invention incorporate a synchronous interface to allow them to be utilized as a conventional memory device. Memory device embodiments of the present invention utilize an external or embedded controller and/or memory buffer to present the high density non-volatile memory device(s) as a conventional memory device having a synchronous interface. This allows the high density non-volatile memory embodiments of the present invention to support in-place code execution and allow them to be booted from. Additionally, the memory buffer allows for caching/buffering of data read and/or write accesses, allowing high density non-volatile memory devices of the present invention to be quickly accessed as if they were conventional synchronous RAM memory devices. In one embodiment of the present invention, a high density non-volatile memory device eliminates the requirement of external drivers, a memory controller, a customized interface port on a microprocessor, and/or operating system support to utilize a specialized high density non-volatile memory device, and in particular, a NAND architecture Flash memory device. This simplifies the use and design effort of high density non-volatile memories by reducing specialized interfacing, while reducing the overall production cost through allowing use of a less expensive NAND architecture Flash memory or other high density non-volatile memory where a more expensive memory device

would normally be required.."). Such features are variously claimed by Applicant in the pending claims.

Applicant therefore contends that Stobbs et al. or Charlier et al., either alone or in combination do not make a prima facie case of anticipation or obviousness against Applicant's pending claims. Accordingly, Applicant contends that the pending claims are patentably distinct from these references.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250